Terminal; of a single inverter 55 whose output terminal is connected to bus 59. Bus 59 is connected to a second output terminal 61 of all AND gates 511.

Initially, there is no sound incident on any of the detectors so that the input signal to all of the gates is zero. When a sound signal is radiated from a sound source, the closest detector is the first to receive the signal and sends a positive signal to one input of its gate. Since the signal on the second terminal is zero (not negative) the first gate to receive it signal from its detector 30 will send a signal to its address register 63. The positive signal from the first gate to receive the sound signal is inverted by inverter 55 and the negative signal is applied through the second bus 59 to the second input terminal of all the remaining gates thereby turning off all remaining gates.

The video memory 40 reads the selected address from register 63 and applies the image data on monitor 42.

An alternate scheme for detecting the direction of sound is shown in fig. 4. [[fig.4.]] There is shown a ring of audial detectors 30 arranged relative to the audial lens. The lens is not shown in fig. 4 but is arranged coaxial with the audial detector array as discussed with regard to fig. 1.

Each detector 30 of the array of detectors forms a pair of detectors with one member of each pair being positioned on a circumferential boundary oppositely from one another member of the pair. For example,
Detectors 30A and 30 B form one pair, detectors 30C and 30 D form another pair. A plurality of difference circuits is provided although only two difference circuits are shown in [[fig. 4. ]] fig. 4: a difference circuit for each pair of detectors, one pair of detectors for each difference circuit 37.

Fig. 4 shows inverters 39 (two are shown).

one inverter for each pair of detectors , one pair of detectors for each inverter;

a rectifiers 49, one rectifier 49 for each pair of detectors 30, one pair of detectors for each rectifier 49;

An address register 41 having a plurality of address input terminals,
one address terminal for one difference circuit and one difference circuit for one address terminal;

One member of each pair of detectors 50 is connected to transmit an image signal to an input terminal of one of the inverters 39;

An output terminal of the inverter is connected to an input terminal of the difference circuits;

another one of the pair of rectifiers has an input terminal connected to an output terminal of the difference circuit 37;

each one of the rectifiers 49 has an input terminal connected to an output terminal of the difference circuit 37;

each one of the rectifiers 49 has an output terminal connected to one of the input terminals of the address register 41;

the address register has an output terminal configured to emit an address signal responsive to a null signal from one of the rectifiers.

The timing diagrams of figs. 3.1 - 3.7 show the signals generated by a sound pulse 46 incident on the array of detectors 30. Detector 30c is the "leading" detector where the phase shift of the incoming wave will be assumed to be zero as shown in [[fig. 3,4]] fig. 3.4. Figs. 3.1 and 3.2 show that the signals received by detectors 30A and 30B have shifted an equal amount, Ø, so that the difference between their signal (fig. 3.3) is zero. The inverted signal, Fig. 3.5, from detector 30D has shifter to 2Ø thereby giving pulse 3.6